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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/847,032	04/30/2001	Lester S. Sanders	X-858 US	5645

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XILINX, INC
ATTN: LEGAL DEPARTMENT
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EXAMINER	
PHAN, THAI Q	

ART UNIT	PAPER NUMBER
2128	

DATE MAILED: 11/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/847,032	SANDERS, LESTER S.	
	Examiner	Art Unit	
	Thai Q. Phan	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 April 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to applicant's amendment to the claims, filed on 07/27/2004. Claims 22-30 are newly added. Claims 1-30 remain pending in the Action.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Balakrishnan et al, US patent no. 6,135,647.

As per claim 1, Balakrishnan discloses a method and system for circuit design and synthesis with feature limitations very similar to the claimed invention. According to Balakrishnan, the design method includes steps:

Receiving a first low level design or design representation for a target circuit (Figs. 3, 4, 5, col. 4, line 61 to col. 5, line 43, for example),

Transforming the first low level design representation into a synthesizable and simulatable HDL high level representation (Figs. 21, 22, col. 5, lines 44-59, col. 6, lines 3-51, for example),

And processing the high level design representation to generate a low-level design representation for a target circuit dependent on technology (col. 10, lines 49-58,

col. 11, lines 21-36, col. 12, lines 21-49, for example). Balakrishnan discloses RTL code translator independent from HDL level for any technology.

Balakrishnan does not expressly disclose a second low level design representation targeting a second integrated circuit as claimed.

It would have been obvious for practitioner in the art at the time of the invention was made to find that Balakrishnan RTL translator for HDL level system would imply the claimed limitation of a second low level design representing targeting a second integrated circuit because the RTL code translates HDL code for a target device independent of technology as disclosed in Balakrishnan above.

As per claims 2-5, Balakrishnan discloses the claimed limitations such as logic devices, gate arrays, programmable logic devices, etc which are called digital devices.

As per claims 6-9, Balakrishnan discloses a plurality of programming languages would be used in ASIC design environment. Such languages would include HDL, VHDL, RTL, etc. to express logic operations or logic functions. Thus, the design language would include other well known languages such as ABEL code as claimed.

As per claim 10, Balakrishnan discloses RTL code translator which would include parsing the low level design representation to generate a synthesizable and simulatable high level code objects which are technology independent for a second target device (col. 4, lines 23-45, col. 6, lines 15-35, for example).

As per claim 11, Balakrishnan discloses digital logic circuit and object component for the related circuit. Such object components could include the claimed flip-flop circuit.

As per claims 12-21, Balakrishnan disclosure is for digital design which would include a plurality of design components as claimed. Balakrishnan also discloses design languages used in the design would include HDL, VHDL, RTL, Verilog, C, etc. This would include other design languages known in the art of digital design such as the claimed ABEL codes.

As per claim 22, Balakrishnan discloses a method and system for circuit design and synthesis with feature limitations very similar to the claimed invention. According to Balakrishnan, the design method includes steps:

Receiving a first low level design or design representation for a target circuit (Figs. 3, 4, 5, col. 4, line 61 to col. 5, line 43, for example),

Transforming the first low level design representation into a synthesizable and simulatable high level representation (col. 5, lines 44-59, col. 6, lines 3-51, col. 12, lines 13-20, for example),

And processing the high level design representation to generate a low-level design representation for a target circuit dependent on technology (col. 10, lines 49-58, col. 11, lines 21-36). Balakrishnan discloses RTL code translator independent from HDL level for any technology design.

Balakrishnan does not expressly disclose a second low level design representation targeting a second integrated circuit as claimed.

It would have been obvious for practitioner in the art at the time of the invention was made to find that Balakrishnan RTL translator for HDL level system would imply the claimed limitation of a second low level design representing targeting a second

integrated circuit because the RTL code translates HDL code for a target device independent of technology as disclosed in Balakrishnan above.

As per claims 23, and 24, Balakrishnan discloses a complex programmable logic device and field programmable logic array for the second type of integrated circuit.

As per claim 25, Balakrishnan discloses an ASIC for the second type of device.

As per claim 26, Balakrishnan discloses HDL programming language in the design.

As per claims 27-28, Balakrishnan discloses logic expression or Boolean expression as claimed (col. 8, lines 27-54, for example).

As per claim 29, Balakrishnan discloses steps identifying equations in the low level design specification having information for synthesizable and simulatable objects and writing to the high level design specification, synthesizable objects using the information from the identified equations.

As per claim 30, Balakrishnan discloses a method and system for circuit design and synthesis with feature limitations very similar to the claimed invention. According to Balakrishnan, the design system includes means:

Receiving a first low level design or design representation for a target circuit (Figs. 3, 4, 5, col. 4, line 61 to col. 5, line 43, for example),

Transforming the first low level design representation into a synthesizable and simulatable high level representation (col. 5, lines 44-59, col. 6, lines 3-51, col. 12, lines 13-20, for example),

And processing the high level design representation to generate a low-level design representation for a target circuit dependent on technology (col. 10, lines 49-58, col. 11, lines 21-36). Balakrishnan discloses RTL code translator independent from HDL level for any technology design.

Balakrishnan does not expressly disclose a second low level design representation targeting a second integrated circuit as claimed.

It would have been obvious for practitioner in the art at the time of the invention was made to find that Balakrishnan RTL translator for HDL level system would imply the claimed limitation of a second low level design representing targeting a second integrated circuit because the RTL code translates HDL code for a target device independent of technology as disclosed in Balakrishnan above.

Response to Arguments

Applicant's arguments with respect to claims 1-30 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

1. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

1. US patent no. 5,673,198, issued to Lawman et al, on Sept. 1997
2. US patent no. 6,226,776 B1, issued to Panchul et al, on May 2001
3. US patent no. 6,243,851 B1, issued to Hwang et al, on June 2001

4. US patent no. 6,691,078 B1, issued to Beer et al, on Feb. 2004

5. US patent application no. US 2002/0069396 A1, publication date June 2002

2. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thai Q. Phan whose telephone number is 571-272-3783.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jean Homere can be reached at 571-272-3780. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

3. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Nov. 10, 2004

Thai Phan
Patent Examiner
AU: 2128